WHAT IS CLAIMED IS:

1. An amplifier, comprising:

a plurality of differential pairs coupled together through a common differential output, each differential pair having a current control input; and

a current switch coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier.

2. The amplifier of claim 1 wherein the differential pairs each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

3. The amplifier of claim 2 wherein the transistors each comprises a field effect transistor

4. The amplifier of claim 3 wherein the first and second transistors in each differential pair each comprises a source coupled to its respective common node.

5. The amplifier of claim 4 wherein the first and second transistors in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

6. The amplifier of claim 3 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output.

7. The amplifier of claim 1 wherein the current switch comprises a transistor.

8 The amplifier of claim 7 wherein the transistor comprises a field effect transistor.

9. The amplifier of claim 8 wherein the transistor comprises a drain coupled to its respective current control input.

10. The amplifier of claim 1 wherein the current switch comprises a current source having a switch control input.

11. The amplifier of claim 10 further comprising a bias circuit coupled to the switch control input.

12. The amplifier of claim 11 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

13. The amplifier of claim 12 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

14. The amplifier of claim 13 wherein the summer comprises a cascode current mirror.

15. The amplifier of claim 12 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

16. The amplifier of claim 1 further comprising a matching circuit coupled to the common differential output.

17. The amplifier of claim 16 wherein the matching circuit converts a differential current from the common differential output to a single-ended current.

18. The amplifier of claim 16 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier.

19. The amplifier of claim 16 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

20. The amplifier of claim 1 wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input.

21. The amplifier of claim 1 further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier.

22. An amplifier, comprising:

a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output, the second nodes of the first transistors being coupled together and the second nodes of the second transistors being coupled together to form a differential input, and the third node of each of the first transistors being coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages; and

a current switch coupled to the current control input of one the amplifying stage to switch said one of the amplifying stages in or out of the amplifier.

23. The amplifier of claim 22 wherein the transistors each comprises a field effect transistor.

24. The amplifier of claim 23 wherein the third nodes each comprises a source.

25. The amplifier of claim 24 wherein the second nodes each comprises a gate.

26. The amplifier of claim 23 wherein the first nodes each comprises a drain.

27. The amplifier of claim 22 wherein the current switch comprises a transistor.

28. The amplifier of claim 27 wherein the transistor comprises a field effect transistor.

29. The amplifier of claim 28 wherein the transistor comprises a drain coupled to its respective current control input.

30. The amplifier of claim 22 wherein the current switch comprises a current source having a switch control input.

31. The amplifier of claim 30 further comprising a bias circuit coupled to the switch control input.

32. The amplifier of claim 31 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied the switch control input.

33. The amplifier of claim 32 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

34. The amplifier of claim 33 wherein the summer comprises a cascode current mirror.

35. The amplifier of claim 34 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

36. The amplifier of claim 22 further comprising a matching circuit coupled to the differential output.

37. The amplifier of claim 36 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

38. The amplifier of claim 36 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

39. The amplifier of claim 36 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

40. The amplifier of claim 22 further comprising an input stage coupled to the differential input.

41. The amplifier of claim 22 further comprising a plurality of current switches each coupled the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

42. An amplifier, comprising:

a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input; and

a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit.

43. The amplifier of claim 42 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

44. The amplifier of claim 43 wherein the transistors each comprises a field effect transistor.

45. The amplifier of claim 44 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

46. The amplifier of claim 45 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

47. The amplifier of claim 44 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

48. The amplifier of claim 42 wherein the current switch comprises a transistor.

49 The amplifier of claim 48 wherein the transistor comprises a field effect transistor.

50. The amplifier of claim 49 wherein the transistor comprises a drain coupled to its respective current control input.

51. The amplifier of claim 42 wherein the current switch comprises a current source having a switch control input.

52. The amplifier of claim 51 further comprising a bias circuit coupled to the switch control inputs.

53. The amplifier of claim 52 wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

54. The amplifier of claim 53 wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

55. The amplifier of claim 54 wherein the summer comprises a cascode current mirror.

56. The amplifier of claim 53 wherein the current source comprises a field effect transistor having a gate comprising the switch control input.

57. The amplifier of claim 42 further comprising a matching circuit coupled to the differential output.

58. The amplifier of claim 57 wherein the matching circuit converts a differential current from the differential output to a single-ended current.

59. The amplifier of claim 57 wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit.

60. The amplifier of claim 57 wherein the differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output

and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

61. The amplifier of claim 42 wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input.

62. The amplifier of claim 22 further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

63. An amplifier comprising a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level.

64. The amplifier of claim 63 wherein the amplifier comprises CMOS.

65. The amplifier of claim 63 further comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input, and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier.

66. The amplifier of claim 65 wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

67. The amplifier of claim 66 wherein the transistors each comprises a field effect transistor.

68. The amplifier of claim 67 wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node.

69. The amplifier of claim 68 wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

70. The amplifier of claim 67 wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

71. The amplifier of claim 65 wherein the current switches each comprises a transistor.

72 The amplifier of claim 71 wherein the transistors each comprises a field effect transistor.

73. The amplifier of claim 72 wherein the transistors each comprises a drain coupled to its respective current control input.

74. The amplifier of claim 65 wherein the current switches each comprises a current source having a switch control input.

75. The amplifier of claim 74 further comprising a plurality of bias circuits each coupled to a different one of the switch control inputs.

76. The amplifier of claim 75 wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input.

77. The amplifier of claim 76 wherein the bias circuits each comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the its respective switch control input.

78. The amplifier of claim 77 wherein the summer comprises a cascode current mirror.

79. The amplifier of claim 76 wherein the current sources each comprises a field effect transistor having a gate comprising the switch control input.

80. An amplifier, comprising:

a plurality of amplifying stages coupled together;

switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier; and

matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power.

81. The amplifier of claim 80 wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input

82. The amplifier of claim 81 wherein the transistors each comprises a field effect transistor.

83. The amplifier of claim 82 wherein the first and second transistors each comprises a source coupled to its respective common node.

84. The amplifier of claim 83 wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input.

85. The amplifier of claim 82 wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output.

86. The amplifier of claim 80 wherein the switching means comprises a transistor.

87 The amplifier of claim 86 wherein the transistor comprises a field effect transistor.

88. The amplifier of claim 87 wherein the transistor comprises a drain coupled to said one of the amplifying stages.

89. The amplifier of claim 80 wherein the switching means comprises a current source having a switch control input.

90. The amplifier of claim 89 further comprising a bias circuit coupled to the switch control input.

91. The amplifier of claim 90 wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input.

92. The amplifier of claim 90 wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input.

93. The amplifier of claim 92 wherein the summer comprises a cascode current mirror.

94. The amplifier of claim 80 wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single-ended current being coupled to the amplifier output.

95. The amplifier of claim 80 wherein the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled to the amplifier output.